In the Claims:

Please cancel claims 1-13, 15-18, 20-22, and 24-25. Please amend claim 14. Please add new claims 27-51. The claims are as follows.

1-13. (Canceled)

14. (Currently amended) An integrated chip package comprising:

a first substrate and a second substrate;

a mask on a surface of at least one of the first and second substrates, wherein the mask includes a plurality of ~~elongated~~ non-circular openings, said openings having an oblong shape, an oval shape, or an elliptical shape, wherein the openings have a first dimension and a second dimension, wherein the first dimension is greater than the second dimension, and wherein the first dimension of the openings is selectively oriented on the substrate in a direction of highest stress within each interconnection; and

a plurality of interconnections between the first and second substrates.

15-26. (Canceled)

27. (New) The integrated chip package of claim 14, wherein the openings have the oblong shape.

28. (New) The integrated chip package of claim 14, wherein the openings have the oval shape.

29. (New) The integrated chip package of claim 14, wherein the openings have the elliptical shape.

30. (New) The integrated chip package of claim 14, further comprising a plurality of traces mounted between the openings of the mask.

31. (New) The integrated chip package of claim 14, wherein the mask comprises a non-wettable material.

32. (New) The integrated chip package of claim 14, wherein the first dimension is oriented in a direction of highest stress within each interconnection.

33. (New) The integrated chip package of claim 14, wherein the mask comprises an epoxy.

34. (New) The integrated chip package of claim 14, wherein the first substrate is a chip carrier, and wherein the second substrate is a printed circuit board.

35. (New) The integrated chip package of claim 34, wherein the mask is on a surface of the chip carrier and not on a surface of the printed circuit board.

36. (New) The integrated chip package of claim 34, wherein the mask is on a surface of the

printed circuit board chip carrier and not on a surface of the chip carrier.

37. (New) The integrated chip package of claim 34, wherein the mask is on a surface of both the chip carrier and the printed circuit board.

38. (New) The integrated chip package of claim 14, wherein the mask is on a surface of both the first substrate and on the second substrate.

39. (New) An integrated chip package comprising a substrate having a plurality of circular conductive pads and a mask thereon, wherein the mask has a plurality of non-circular openings having a first dimension larger than a diameter of the conductive pad, and a second dimension smaller than the diameter of the conductive pad.

40. (New) The integrated chip package of claim 39, wherein the openings having an oblong shape, an oval shape, or an elliptical shape.

41. (New) The integrated chip package of claim 39, wherein the openings have the oblong shape.

42. (New) The integrated chip package of claim 39, wherein the openings have the oval shape.

43. (New) The integrated chip package of claim 39, wherein the openings have the elliptical shape.

44. (New) The integrated chip package of claim 39, further comprising a plurality of traces mounted between the openings of the mask.

45. (New) The integrated chip package of claim 39, wherein the mask comprises a non-wettable material.

46. (New) The integrated chip package of claim 39, wherein the first dimension is oriented in a direction of highest stress within each interconnection formed within the openings of the mask.

47. (New) The integrated chip package of claim 39, wherein the mask comprises an epoxy.

48. (New) The integrated chip package of claim 39, wherein the first substrate is a chip carrier.

49. (New) The integrated chip package of claim 39, wherein the first substrate is a printed circuit board.

50. (New) The integrated chip package of claim 39, further comprising interconnections formed within the openings of the mask.

51. (New) The integrated chip package of claim 50, wherein the interconnections are solder balls that wet only to an area of the conductive pads exposed by the openings in the mask.